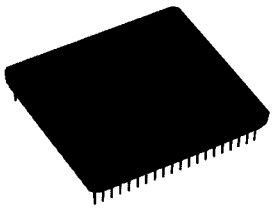
DDC
ILC DATA DEVICE CORPORATION

BUS-65142® AND BUS-65144®

MIL-STD-1553 DUAL REDUNDANT REMOTE TERMINAL HYBRID



APPROX. ½ ACTUAL SIZE

NEW

FEATURES

- LOW POWER & LOW COST
- HIGH RELIABILITY
- SOS & BIPOLAR
- SUPPORTS ALL 13 MODE CODES
- MODE CODE/COMMAND WORD ILLEGALIZATION
- DMA TRANSFERS
- CONTINUOUS SELF-TEST
- SEAFAC TESTED COMPONENTS
- BUILT-IN-TEST WORD REGISTER
- 16MHz DECODERS OFFER IMPROVED NOISE REJECTION & ZERO CROSSING DETECTION

DESCRIPTION

The BUS-65142 is a complete dual redundant MIL-STD-1553 Remote Terminal Unit (RTU) packaged in a small 1.9" x 2.1" hybrid. The device is based upon two DDC custom ICs, which includes two monolithic low power Mark II transceivers and one CMOS-SOS RTU protocol containing data buffers and timing control logic. It supports all 13 mode codes for dual redundant operation, any combination of which can be illegalized.

Parallel data transfers are accomplished with a DMA type handshaking, compatible with most CPU types. Data transfers to/from memory are simplified by the latched command word and word count outputs. Error detection and recovery are enhanced by BUS-65142 special features. A 14 bit built-in-test word register stores RTU information, and sends it to the Bus Controller in response to the Mode Command Transmit Bit Word. The BUS-65142 performs continuous on-line wrap-around self-test, and provides 4 error flags to the host CPU. Inputs are provided for host CPU control of 6 bits of the RTU Status Word.

Its small hermetic package, −55°C to +125°C operating temperature range, and complete RTU operation make the BUS-65142 ideal for most MIL-STD-1553 applications requiring hardware or microprocessor subsystems.

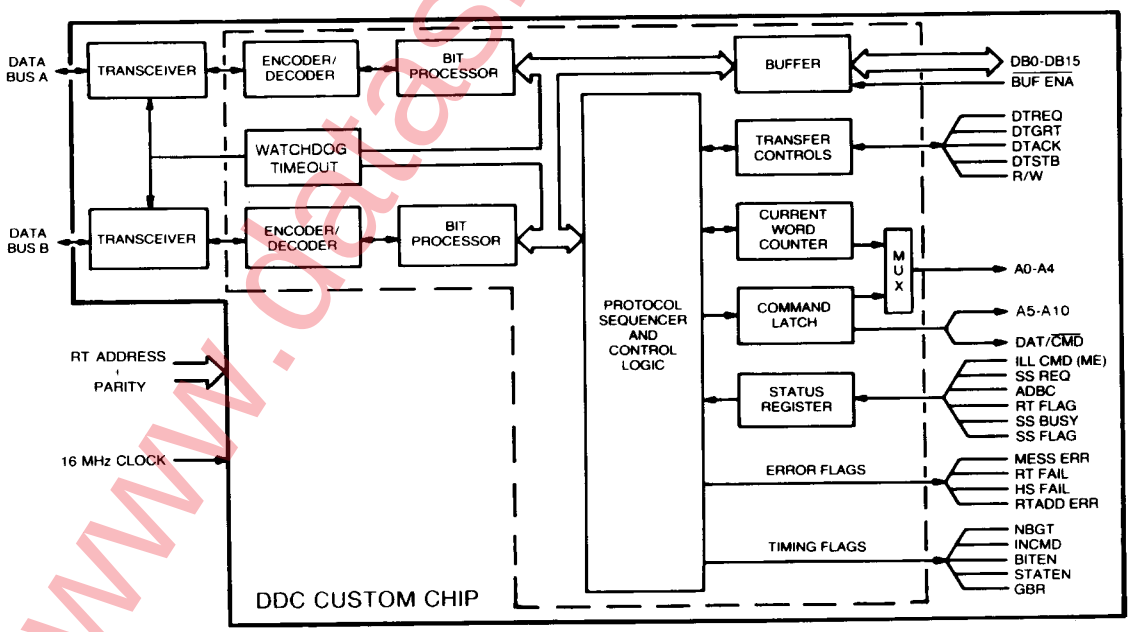


FIGURE 1. BUS-65142 BLOCK DIAGRAM

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SPECIFICATIONS			
PARAMETER	**UNITS**	**VALUE**	
RECEIVER			
Differential Input Impedance (DC to 1 MHz)	kΩ	4 min	
Differential Input Voltage	V_{p-p}	40 max	
Input Threshold (Direct Coupled)	V_{p-p}	0.70 min, 1.20 max	
CMRR (DC to 2 MHz)	dB	40 min	
CMV (DC to 2 MHz)	V	±10 min	
TRANSMITTER			
Differential Output Voltage			
Direct Coupled (Across 145Ω Load)	V_{p-p}	30 typ	
Transformer Coupled (at Stub)	V_{p-p}	21 typ	
Output Rise and Fall Times (Note 7)	ns	160 typ	
Output Noise	mV_{p-p}	10 max	
LOGIC			
V_{IH}	V	2.4 min	
V_{IL}	V	0.7 max	
I_{IH} (Note 1 & 6)(V_{IH}=2.7V)	mA	0.04 min, 0.2 max	
I_{IH} (Note 2)(V_{IH}≥2.4V)	μA	±20 max	
I_{IL} (Note 1 & 6)(V_{IL}=0.4V)	mA	−0.4 max	
I_{IL} (Note 2)(V_{IL}≥0.7V)	μA	±20 max	
V_{OH} (Note 3)(I_{OH}=−0.4mA)	V	2.4 min	
V_{OH} (Note 4)(I_{OH}=−0.4mA)	V	2.4 min	
V_{OH} (Note 6)(I_{OH}=−0.4mA)	V	2.4 min	
V_{OL} (Note 3)(I_{OL}=−2mA)	V	0.4 max	
V_{OL} (Note 5)(I_{OL}=−2mA)	V	0.4 max	
V_{OL} (Note 6)(I_{OL}=−4mA)	V	0.4 max	
C_I (f=1 MHz)	pF	50 max	
C_O (f=1 MHz)	pF	10 typ	
C_{IO} (Note 6) (f=1 MHz)	pF	50 max	
POWER SUPPLIES (TOTAL HYBRID)		**65142**	**65143**
+5VDC			
Tolerance, max	%	±10	±10
Current Drain, max	mA	115	115
−15VDC or −12VDC			
Tolerance, max	%	±5	±5
Current Drain (Note 8)			
Idle, max	mA	70	70
50% Transmit, max	mA	175	185
100% Transmit, max	mA	270	305
TEMPERATURE RANGE			
Operating (Case)	°C	−55 to +125	
Storage	°C	−65 to +150	
PHYSICAL			
Size			
DDIP	in. (mm)	1.9 x 2.1 x 0.25 (48 x 53 x 6)	
Flatpack	in. (mm)	1.6 x 2.19 x 0.171 (40.6 x 55.6 x 4.34)	
Weight	oz(g)	1.7(41)	

Notes:

1. I_{IH} and I_{IL} for input pins 12, 13, 14, 15, 53, 54, 55 (30kΩ pull-ups).
2. I_{IH} and I_{IL} for input pins other than in Note 1.
3. V_{OH} and V_{OL} for output pins 1, 2, 3, 16, 25, 27, 28, 35, 40, 41, 42, 65, 73, 78.
4. V_{OH} for all output pins other than in Note 3.
5. V_{OL} for output pins 21, 22, 24, 26, 29, 60, 61, 62, 63, 64.
6. V_{OL} and C_{IO} for pins 43 thru 50 and 4 thru 11 (45kΩ pull-ups).
7. 120ns min, 200ns max
8. Measured at 5.5V; -15.75V

GENERAL

The BUS-65142 is a complete dual redundant Remote Terminal Unit (RTU) packaged in a small 1.9"x2.1" hybrid. It is fully compliant with MIL-STD-1553B and supports all message formats. As shown in Figure 1, it includes 2 transceivers and a custom chip containing 2 encoders, 2 bit processors, an RTU protocol sequencer and control logic, output latches, and buffers. With the addition of 2 data bus transformers (DDC P/N BUS-25679), BUS-65142 is ready to connect to the MIL-STD-1553 data bus.

Data is transferred to and from the subsystem host CPU over a 16 bit parallel highway, which is isolated by a set of bi-directional buffers. All transfers are made with a DMA type handshaking of request, grant, and acknowledge. Read/write and data strobes are provided to simplify interfacing to external RAM. Also simplifying the RAM interface is the availability of latched command word and an auto-incrementing word counter. These signals may be used as an address to map the data directly to and from RAM.

BUS-65142 allows the subsystem host CPU to control 6 of the bits in the RTU status word. Of particular interest is the Illegal Command input which may be used to set the message error bit and illegalize any command word. Four error flags are provided to the subsystem host CPU by the BUS-65142, to aid in assessing its condition. In addition, a continuous on-line self-test is performed by the BUS-65142 on every transmission. The last Transmitted Word of each message is wrapped around the decoder and compared against the Actual Word. Any discrepancy is flagged as an error.

TIMING

The subsystem host CPU interface to the BUS-65142 is simple and compatible with most microprocessors. Figures 3 and 4 illustrate typical MIL-STD-1553 messages of transmit data and receive data, and figures 5 and 6 show RT to RT transfers. In each case, $\overline{\text{NBGT}}$ identifies the start of the message, and INCMD identifies that a command is being processed. The handshake sequence $\overline{\text{DTREQ}}$, $\overline{\text{DTGRT}}$, and $\overline{\text{DTACK}}$ is used to transfer each word over the parallel data highway. $\overline{\text{DTSTR}}$ and R/$\overline{\text{W}}$ are used to control transfers to RAM memory. $\overline{\text{GBR}}$ identifies a "good block received", when a received message has passed all validation checks and has the correct word count. Buffer enable ($\overline{\text{BUFENA}}$) must be applied to enable the internal three-state buffers.

ERROR FLAGS

Four error flags are outputted to the subsystem to provide information on the condition of the BUS-65142. The Message Error ($\overline{\text{ME}}$) line goes LOW if any of the following error conditions exist: format error, word count error, invalid word, sync error, RT to RT address error or T/R bit error. The Remote Terminal Failure ($\overline{\text{RT FAIL}}$) line goes LOW whenever the results of the continuous wraparound self-test shows a discrepancy, or the transmitter watchdog timeout has occurred. The Handshake Failure ($\overline{\text{HS FAIL}}$) line goes LOW whenever the subsystem has not responded to a $\overline{\text{DTREQ}}$ request soon enough with a $\overline{\text{DTGRT}}$ grant. The RT Address Error ($\overline{\text{RTAD ERR}}$) line goes LOW whenever the sum of the 5 address lines and parity lines show a parity error (the terminal will not respond to commands while this error condition exists).

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STATUS REGISTER

Six inputs to the BUS-65142 allow the subsystem host CPU to control bits in the RTU Status Word. The Illegal Command input may be used to set the Message Error bit in the Status Word and suppress the transmission of data to the bus controller. This line is particularly useful in illegalizing any combination of commands. The latched Command Word may be connected to the address pins which lead to an optional external PROM, that would drive the Illegal Command input LOW when it identifies a command that is programmed to be illegal.

The Subsystem Request ($\overline{SRQ}$) line is used to set the service request bit in the Status Word. The Accept Dynamic Bus Control ($\overline{ADBC}$) line is used to set the Bus Control acceptance bit in the Status Word, if that mode command was sent. The Remote Terminal Flag ($\overline{RT\ FLAG}$) line is used to set the terminal flag bit in the Status Word. The Subsystem Busy ($\overline{BUSY}$) line is used to set the busy bit in the Status Word, and to inhibit requests for data from the subsystem. The Subsystem Flag ($\overline{SS\ FLAG}$) line is used to set subsystem flag (fault) bit in the Status Word.

BUILT-IN-TEST WORD

The BUS-65142 contains a 14 bit Built-In-Test (BIT) word register which stores information about the condition of the Remote Terminal. When a Mode Command is received to transmit BIT word, the contents of this register are transmitted over the 1553 data bus. Figure 2 shows the meaning of each bit in the BIT register. Information is included regarding transmitter timeouts, loop test failures, transmitter shutdown, subsystem handshake failure, and the results of individual message validations.

MODE CODES

The BUS-65142 implements all mode codes applicable to dual-redundant systems. Mode codes can also be illegalized using the appropriate I/O signals. Mode command illegalization and handling are detailed in the RTU Operation section and listed in table 2.

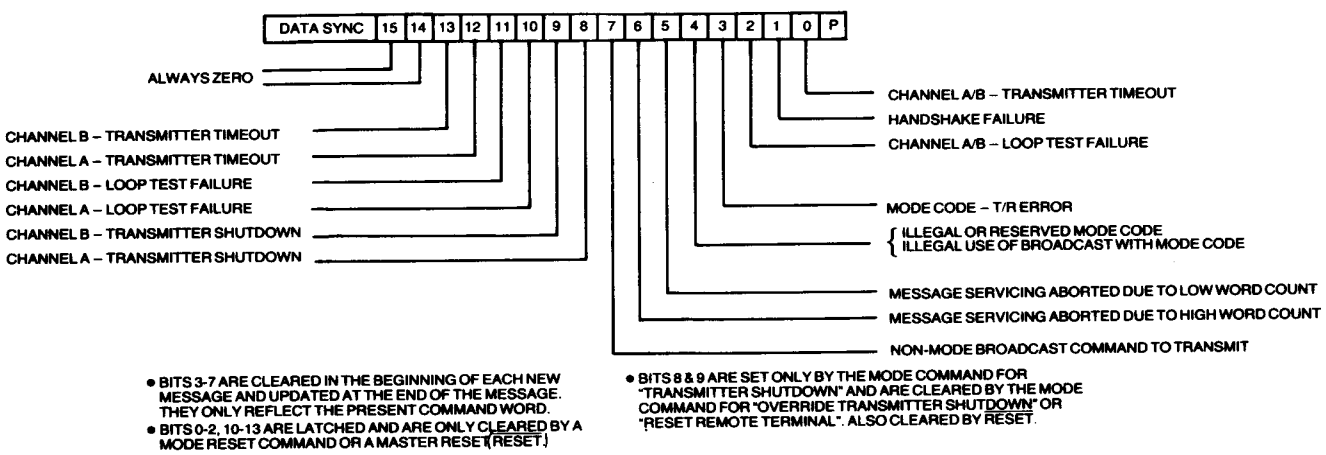

FIGURE 2. BUILT-IN-TEST (BIT) WORD REGISTER

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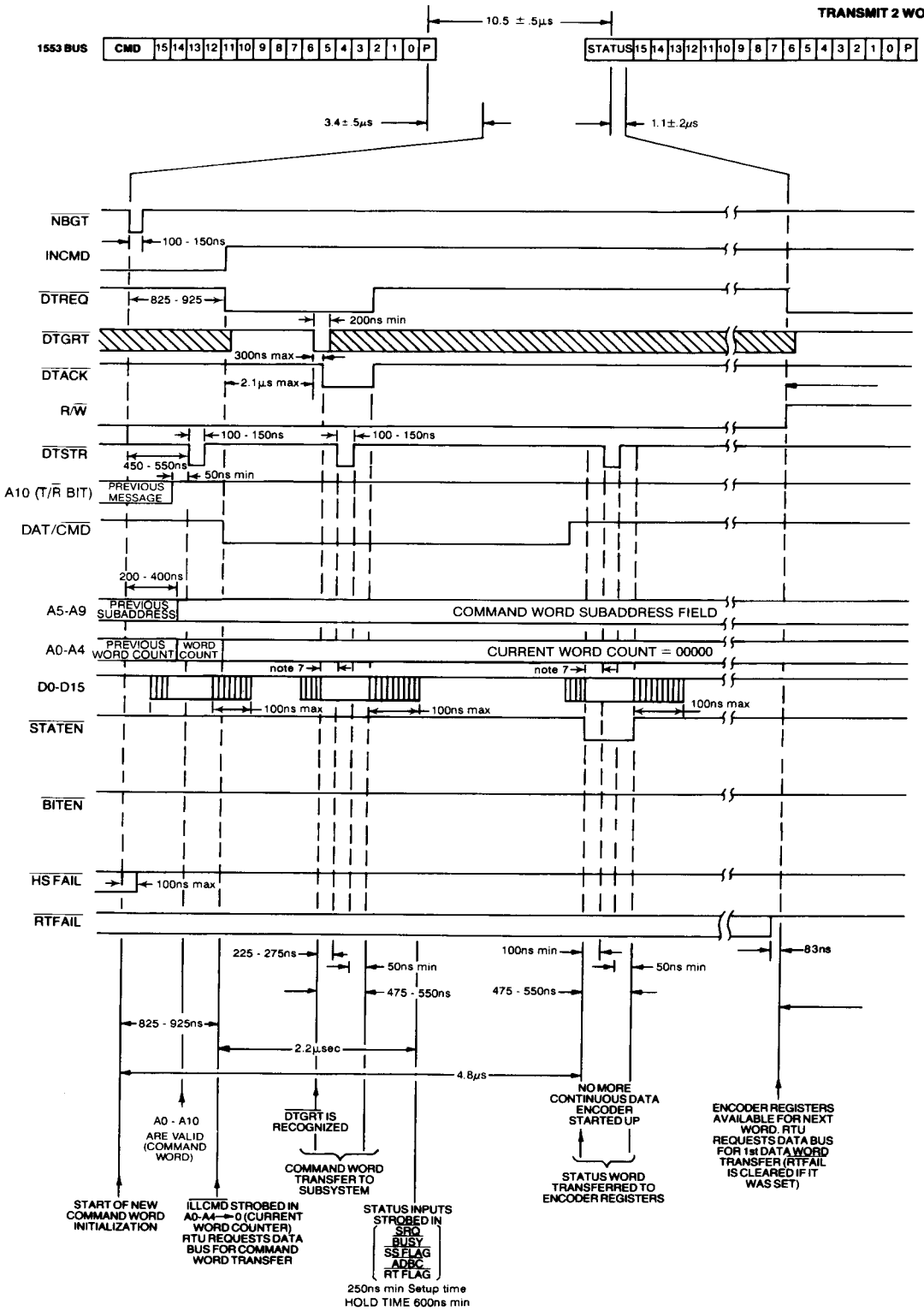

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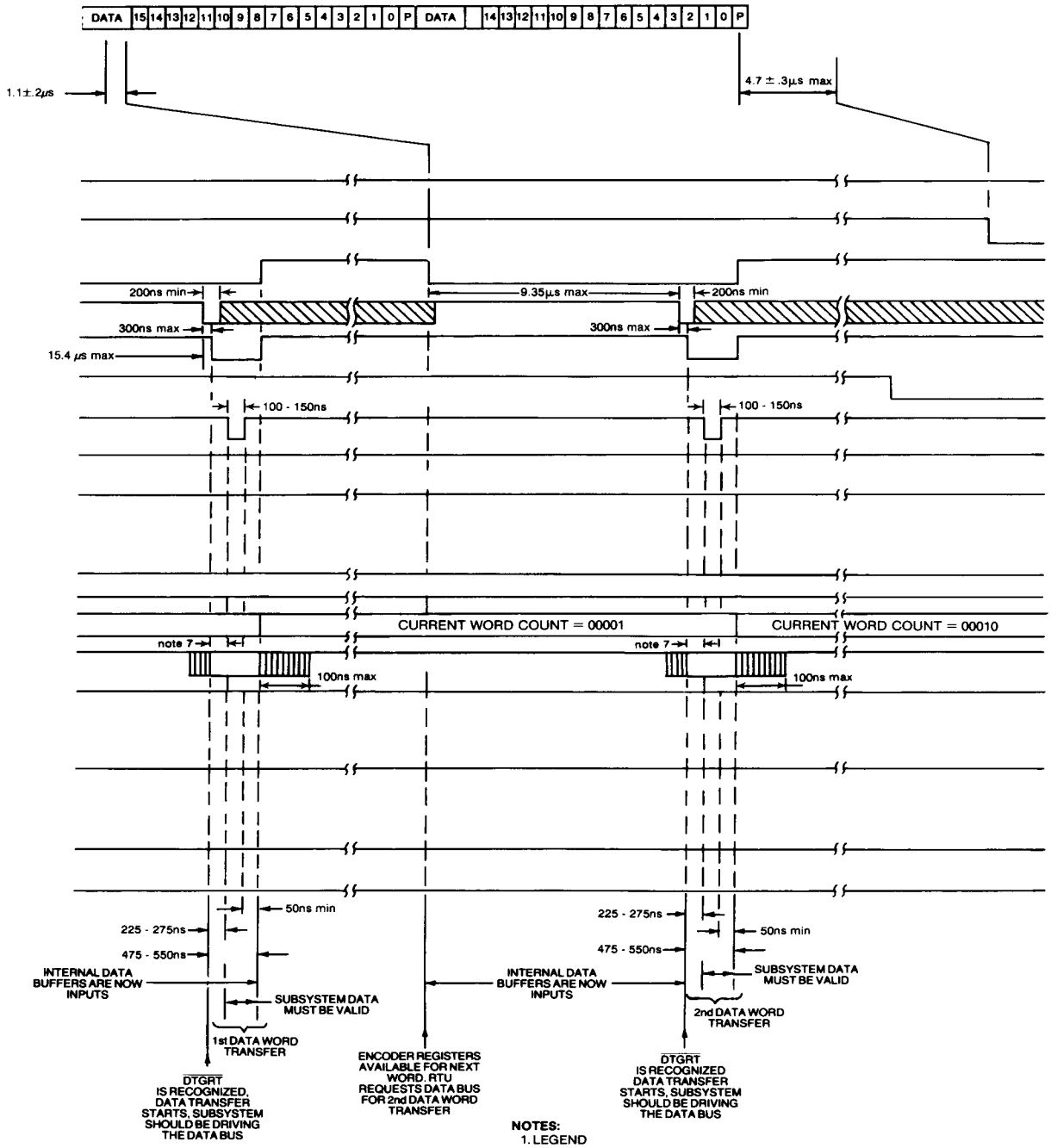

NOTES:

1. LEGEND
   - ▨ DON'T CARE
   - ▥ DATA BUS IS UNDEFINED
2. EACH WORD IS DRIVEN FOR ≈18-19μs ON D0-D15 IF $\overline{\text{BUF ENA}}$ IS ACTIVE – THE LAST WORD IS AVAILABLE FOR 3.5 TO 4 μs SINCE THE STATUS WORD MUST BE SUPPORTED.
3. DATA BUS IS SHOWN WITH $\overline{\text{BUF ENA}}$ CONNECTED TO $\overline{\text{DTACK}}$ (SEE PIN FUNCTION TABLE, PIN 67 ON PAGE 16)
4. THE POSITION OF $\overline{\text{DTACK}}$ WILL VARY DEPENDING ON WHEN $\overline{\text{DTGRT}}$ IS GIVEN. THE MINIMUM TIME WILL BE 166ns FROM $\overline{\text{DTREQ}}$.
5. $\overline{\text{HSFAIL}}$ IS ASSERTED UPON EXCESS $\overline{\text{DTGRT}}$ RESPONSE TIME. INCMD WILL SUBSEQUENTLY GO LOW AND NO FURTHER WORD TRANSFERS WILL OCCUR.
6. $\overline{\text{RTFAIL}}$ IS CLEARED UPON STATUS WORD TRANSMISSION. ONCE SET, FLAG WILL REMAIN SET FOR ENTIRE MESSAGE. INCMD FALLING EDGE CAN BE USED TO LATCH $\overline{\text{RTFAIL}}$ STATUS.
7. 100ns min – REPRESENTS SETUP TIME OF VALID DATA BEFORE THE $\overline{\text{DTSRB}}$ GOES LOW

FIGURE 3. TRANSMIT TIMING DIAGRAM

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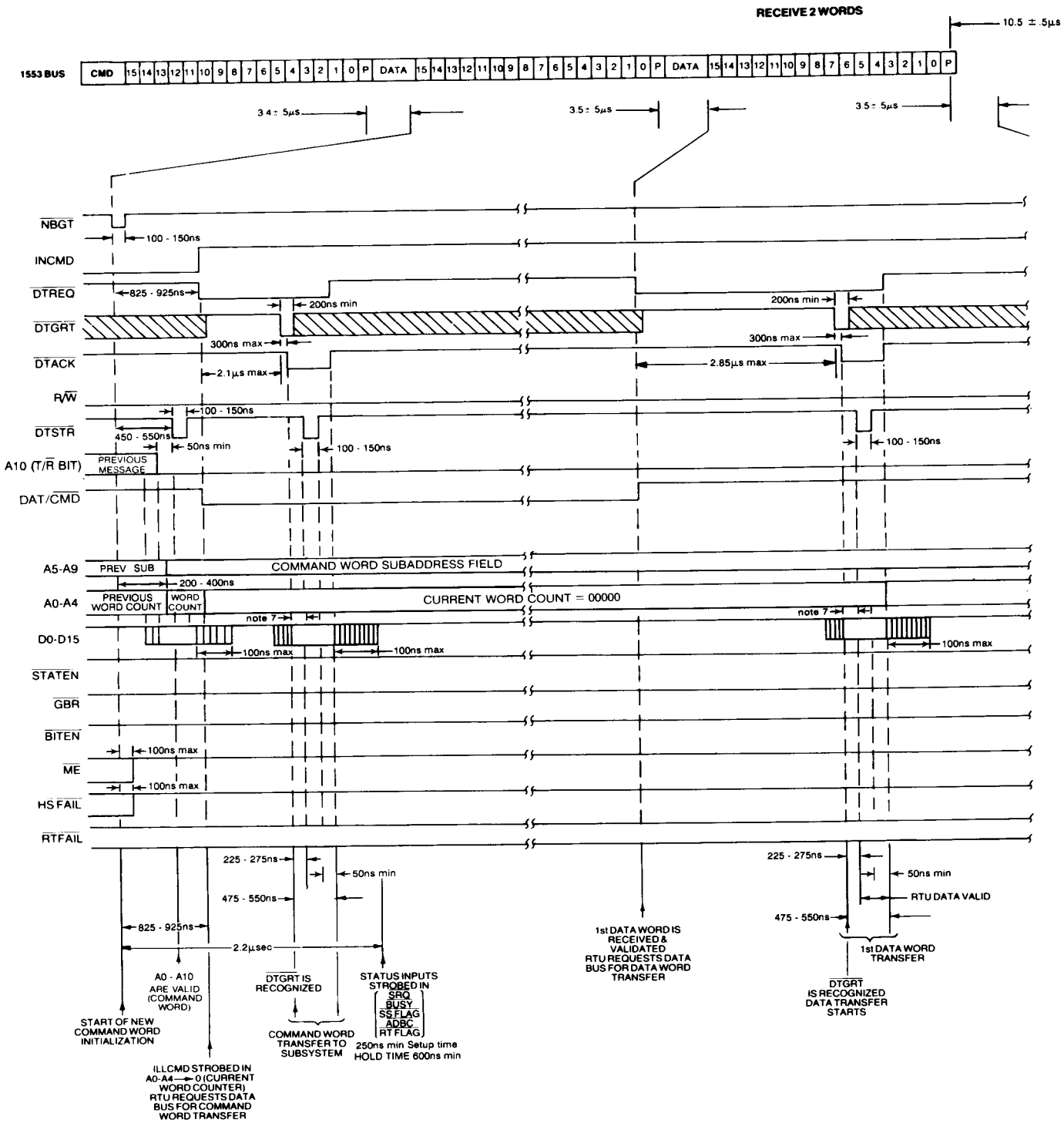

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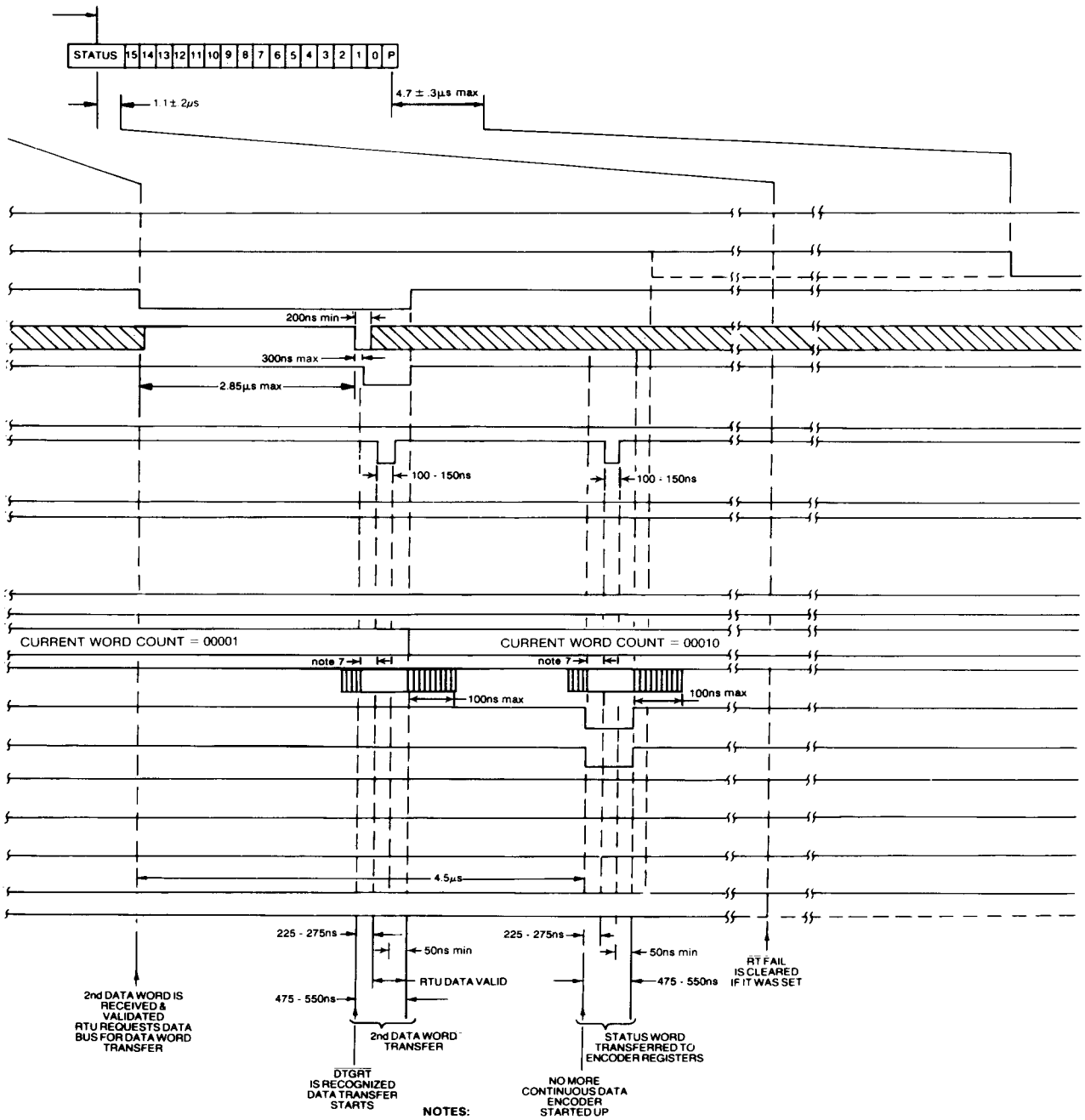

NOTES:

1. LEGEND
   - ▨ DON'T CARE
   - ▥ DATA BUS IS UNDEFINED
   - - - - REPRESENTS THE SEQUENCE OF EVENTS IF THE COMMAND WAS BROADCAST. NOTE, NO STATUS WOULD BE TRANSMITTED ON 1553 BUS
2. EACH WORD IS DRIVEN FOR ≈ 18-19μs ON D0-D15 IF $\overline{\text{BUF ENA}}$ IS ACTIVE – THE LAST WORD IS AVAILABLE FOR 3.5 TO 4 μs SINCE THE STATUS WORD MUST BE SUPPORTED.
3. DATA BUS IS SHOWN WITH $\overline{\text{BUF ENA}}$ CONNECTED TO $\overline{\text{DTACK}}$ (SEE PIN FUNCTION TABLE, PIN 67 ON PAGE 16)
4. THE TIMING DIAGRAMS REPRESENT A DTGRT RESPONSE TIME OF .92μs FOR COMMAND TRANSFER AND 2.1μs FOR DATA. THE POSITION OF $\overline{\text{DTACK}}$ WILL VARY DEPENDING ON WHEN $\overline{\text{DTGRT}}$ IS GIVEN.
5. $\overline{\text{HSFAIL}}$ IS ASSERTED UPON EXCESS $\overline{\text{DTGRT}}$ RESPONSE TIME. $\overline{\text{GBR}}$ WILL BE SET
6. $\overline{\text{RTFAIL}}$ IS CLEARED UPON STATUS WORD TRANSMISSION. ONCE SET, FLAG WILL REMAIN SET FOR ENTIRE MESSAGE. INCMD FALLING EDGE CAN BE USED TO LATCH $\overline{\text{RTFAIL}}$ STATUS.
7. 100ns min – REPRESENTS SETUP TIME OF VALID DATA BEFORE THE $\overline{\text{DTSRB}}$ GOES LOW

FIGURE 4. RECEIVE TIMING DIAGRAM

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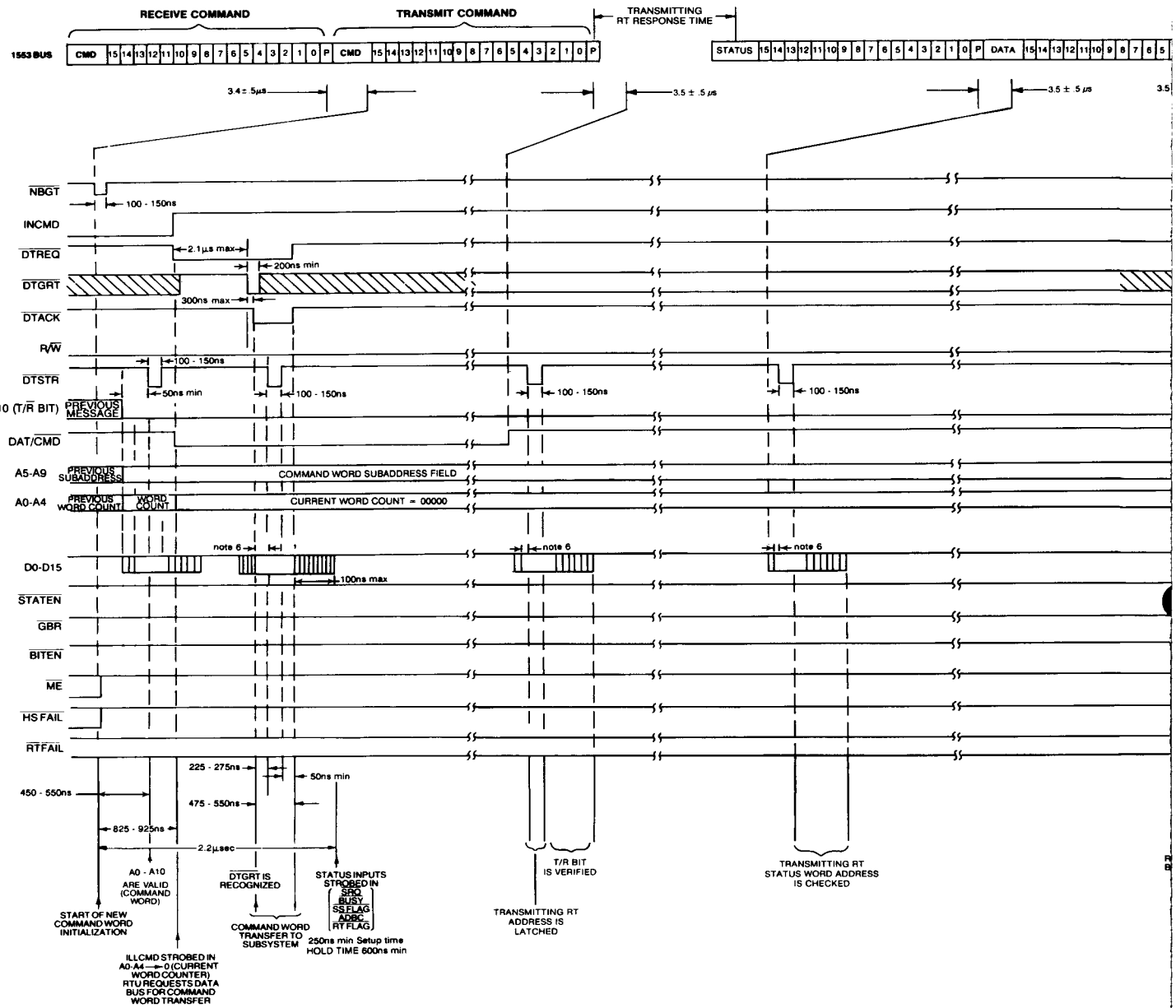

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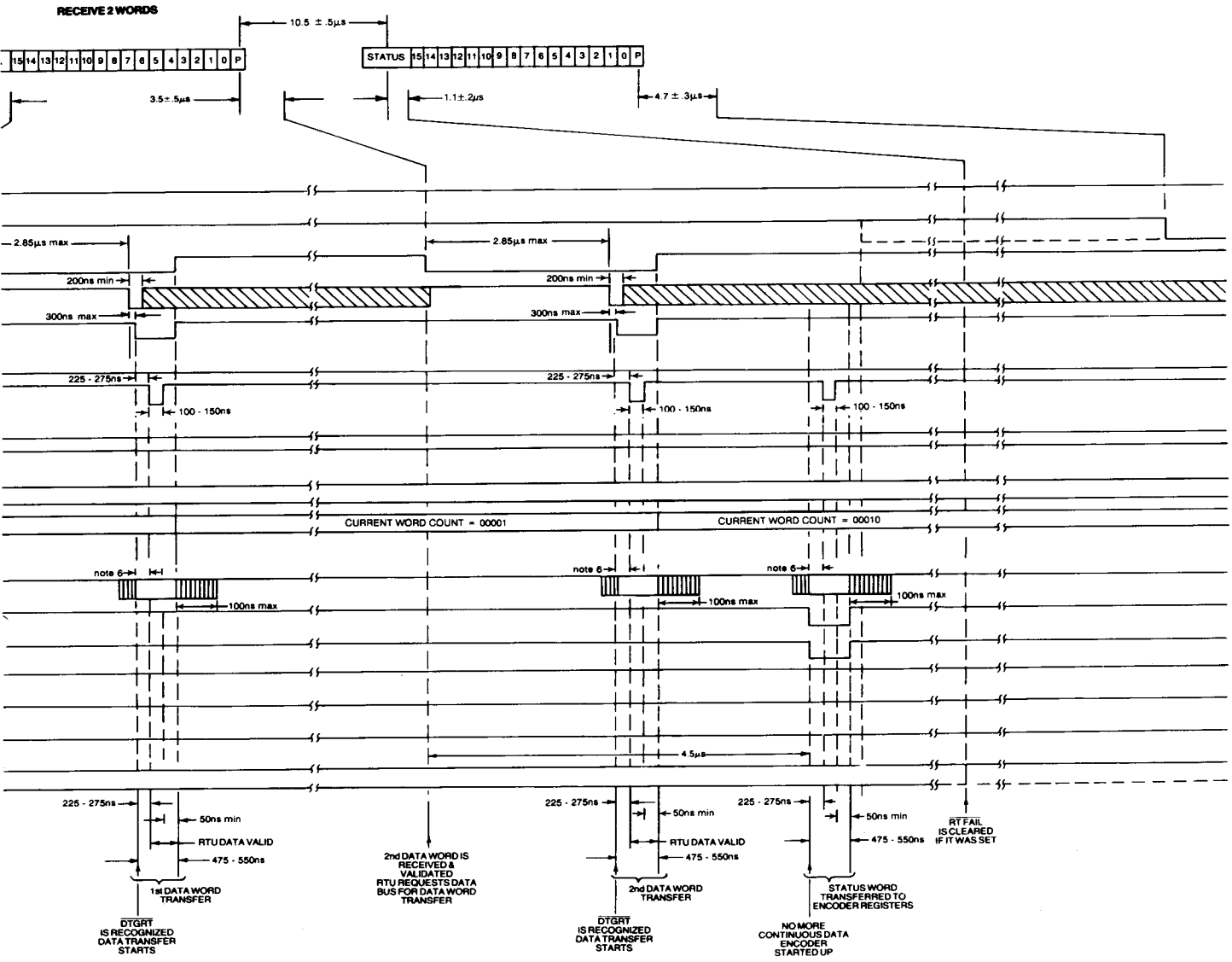

NOTES:

1. LEGEND
   - ▨ DON'T CARE
   - ▥ DATA BUS IS UNDEFINED
   - ---- REPRESENTS THE SEQUENCE OF EVENTS IF THE COMMAND WAS BROADCAST. NOTE, NO STATUS WOULD BE TRANSMITTED ON 1553 BUS.
2. EACH WORD IS DRIVEN FOR ≈18-19µs ON D0-D15 IF $\overline{\text{BUF ENA}}$ IS ACTIVE – THE LAST WORD IS AVAILABLE FOR 3.5 TO 4 µs SINCE THE STATUS WORD MUST BE SUPPORTED.
3. DATA BUS IS SHOWN WITH $\overline{\text{BUF ENA}}$ CONNECTED TO $\overline{\text{DTACK}}$ (SEE PIN FUNCTION TABLE, PIN 67 ON PAGE 16)
4. THE TIMING DIAGRAMS REPRESENT A $\overline{\text{DTGRT}}$ RESPONSE TIME OF .92µs FOR COMMAND TRANSFER AND 2.1µs FOR DATA. THE MAXIMUM RESPONSE TIME FROM $\overline{\text{DTREQ}}$ TO $\overline{\text{DTGRT}}$ TO GUARANTEE A SUCCESSFUL TRANSFER IS 1.5µs FOR THE COMMAND TRANSFER AND 2.33µs FOR DATA TRANSFERS TO THE SUBSYSTEM. THE POSITION OF $\overline{\text{DTACK}}$ WILL VARY DEPENDING ON WHEN $\overline{\text{DTGRT}}$ IS GIVEN.
5. $\overline{\text{RTFAIL}}$ IS CLEARED UPON STATUS WORD TRANSMISSION. ONCE SET, FLAG WILL REMAIN SET FOR ENTIRE MESSAGE. INCMD FALLING EDGE CAN BE USED TO LATCH $\overline{\text{RETFAIL}}$ STATUS.
6. 100ns min – REPRESENTS SETUP TIME OF VALID DATA BEFORE THE $\overline{\text{DTSRB}}$ GOES LOW

FIGURE 5. RT TO RT (RECEIVE) TIMING DIAGRAM

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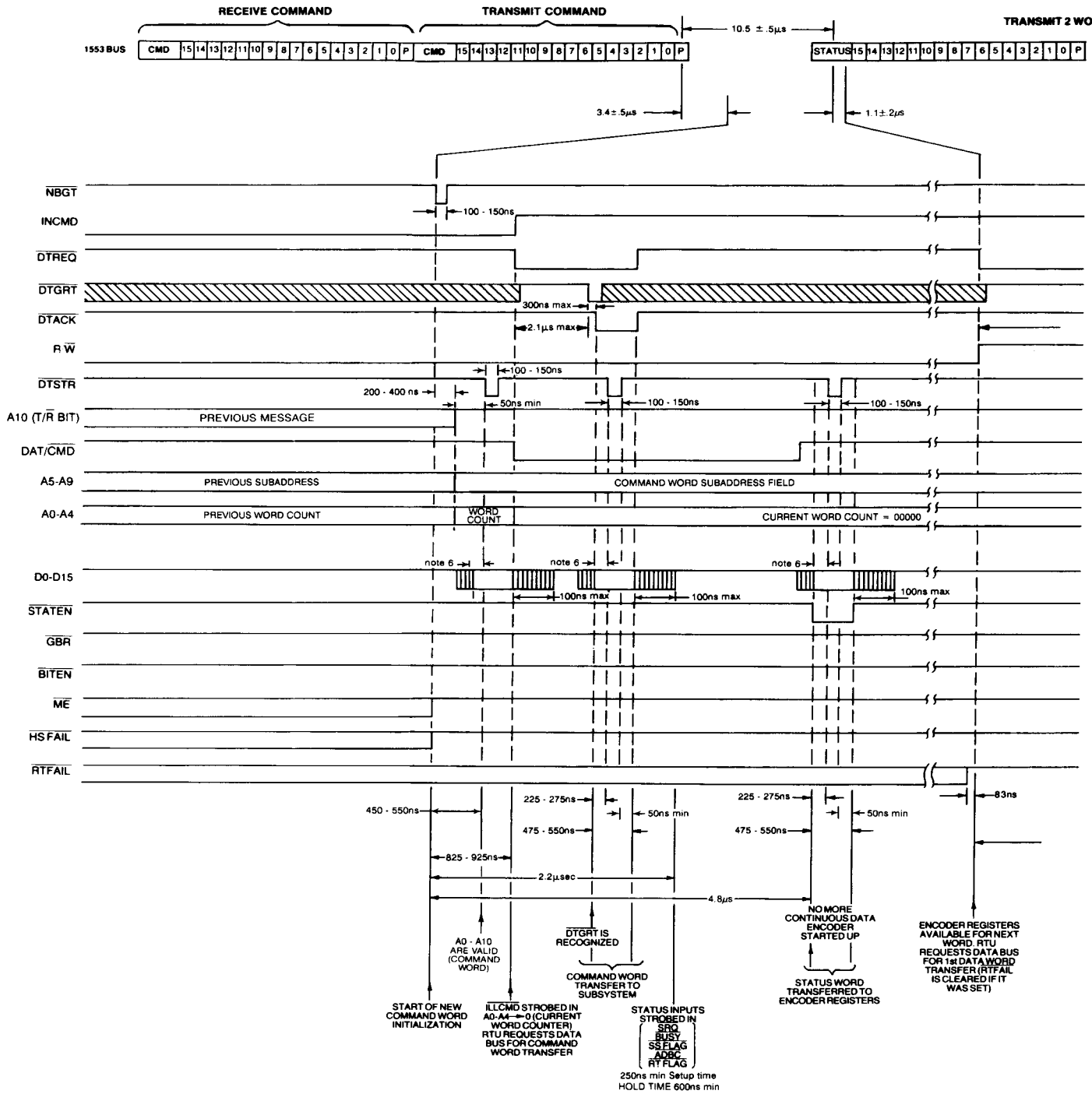

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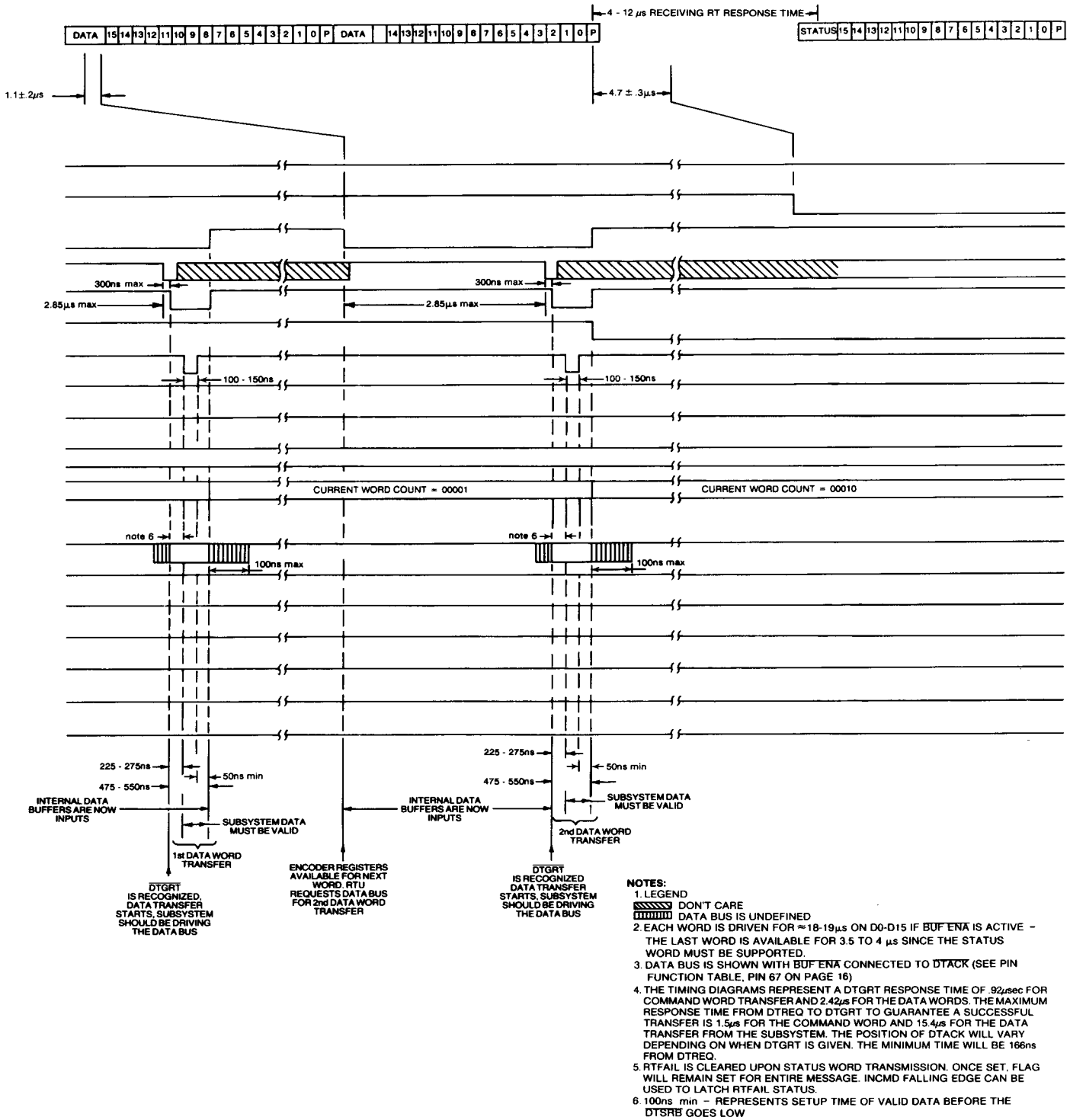

NOTES:

1. LEGEND
   - DON'T CARE
   - DATA BUS IS UNDEFINED
2. EACH WORD IS DRIVEN FOR ≈18-19μs ON D0-D15 IF $\overline{\text{BUF ENA}}$ IS ACTIVE – THE LAST WORD IS AVAILABLE FOR 3.5 TO 4 μs SINCE THE STATUS WORD MUST BE SUPPORTED.
3. DATA BUS IS SHOWN WITH $\overline{\text{BUF ENA}}$ CONNECTED TO $\overline{\text{DTACK}}$ (SEE PIN FUNCTION TABLE, PIN 67 ON PAGE 16)
4. THE TIMING DIAGRAMS REPRESENT A DTGRT RESPONSE TIME OF .92μsec FOR COMMAND WORD TRANSFER AND 2.42μs FOR THE DATA WORDS. THE MAXIMUM RESPONSE TIME FROM DTREQ TO DTGRT TO GUARANTEE A SUCCESSFUL TRANSFER IS 1.5μs FOR THE COMMAND WORD AND 15.4μs FOR THE DATA TRANSFER FROM THE SUBSYSTEM. THE POSITION OF DTACK WILL VARY DEPENDING ON WHEN DTGRT IS GIVEN. THE MINIMUM TIME WILL BE 166ns FROM DTREQ.
5. RTFAIL IS CLEARED UPON STATUS WORD TRANSMISSION. ONCE SET, FLAG WILL REMAIN SET FOR ENTIRE MESSAGE. INCMD FALLING EDGE CAN BE USED TO LATCH RTFAIL STATUS.
6. 100ns min – REPRESENTS SETUP TIME OF VALID DATA BEFORE THE $\overline{\text{DTSRB}}$ GOES LOW

FIGURE 6. RT TO RT (TRANSMIT) TIMING DIAGRAM

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TABLE 2. MODE CODES

DYNAMIC BUS CONTROL (00000)

MESSAGE SEQUENCE = DBC ⋆ STATUS

The BUS-65142 responds with status. If the subsystem wants control of the bus, it must set DBACC within the Configuration Register.

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Followed by Data Word.*** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. ***T/$\overline{R}$ bit Set to Zero.*** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. ***Zero T/$\overline{R}$ bit and Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).
5. ***Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code (BIT Word).

SYNCHRONIZE WITHOUT DATA WORD (00001)

MESSAGE SEQUENCE = SYNC ⋆ STATUS

The BUS-65142 responds with status. If sent as a broadcast, the broadcast receive bit will be set and status response suppressed.

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Followed by Data Word.*** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. ***T/$\overline{R}$ bit Set to Zero.*** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. ***Zero T/$\overline{R}$ bit and Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).

TRANSMIT STATUS WORD (00010)

MESSAGE SEQUENCE = TRANSMIT STATUS ⋆ STATUS

The status and BIT word registers are not altered by this command and contain the resulting status from the previous command.

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Followed by Data Word.*** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. ***T/$\overline{R}$ bit Set to Zero.*** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. ***Zero T/$\overline{R}$ bit and Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).
5. ***Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).

INITIATE SELF-TEST (00011)

MESSAGE SEQUENCE = SELF-TEST ⋆ STATUS

The BUS-65142 responds with a status word. If the command was broadcast, the broadcast received bit is set and status transmission suppressed. Short-loop test is initiated on the status word transmitted. If the test fails, an RT fail flag is set.

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Followed by Data Word.*** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. ***T/$\overline{R}$ bit Set to Zero.*** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. ***Zero T/$\overline{R}$ bit and Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), T/R Error (BIT Word).
5. ***Faulty Test.*** Bits set: terminal flag (SW), A/$\overline{B}$ Loop Test Fail, Current 1553 Bus (A or B) Loop Test Fail (BIT Word).

TRANSMITTER SHUTDOWN (00100)

MESSAGE SEQUENCE = SHUTDOWN ⋆ STATUS

This command is only used with dual redundant bus systems. The BUS-65142 responds with status. At the end of the status transmission, the BUS-65142 inhibits any further transmission from the dual redundant channel. Once shutdown, the transmitter can only be reactivated by Override Transmitter Shutdown or RESET RT commands.

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Followed by Data Word.*** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. ***T/$\overline{R}$ bit Set to Zero.*** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. ***Zero T/$\overline{R}$ bit and Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).

⋆ = Status response time

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TABLE 2. MODE CODES (CONTINUED)

OVERRIDE TRANSMITTER SHUTDOWN (00101)

MESSAGE SEQUENCE = OVERRIDE SHUTDOWN ⋆ STATUS

This command is only used with dual redundant bus systems. The BUS-65142 responds with status. At the end of the status transmission, the BUS-65142 re-enables the transmitter of the redundant bus. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Followed by Data Word.*** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. ***T/$\overline{R}$ bit Set to Zero.*** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. ***Zero T/$\overline{R}$ bit and Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error (BIT Word).

INHIBIT TERMINAL FLAG BIT (00110)

MESSAGE SEQUENCE = INHIBIT TERMINAL FLAG ⋆ STATUS

The BUS-65142 responds with status and inhibits further internal or external setting of the terminal flag bit in the status register. Once the terminal flag has been inhibited, it can only be reactivated by an Override Inhibit Terminal Flag or Reset RT command. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Followed by Data Word.*** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. ***T/$\overline{R}$ bit Set to Zero.*** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. ***Zero T/$\overline{R}$ bit and Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), T/R Error (BIT Word).

OVERRIDE INHIBIT TERMINAL FLAG BIT (00111)

MESSAGE SEQUENCE = OVERRIDE INHIBIT TERMINAL FLAG ⋆ STATUS

The RTU responds with status and reactivates the terminal flag bit in the status register. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Followed by Data Word.*** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. ***T/$\overline{R}$ bit Set to Zero.*** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. ***Zero T/$\overline{R}$ bit and Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), T/R Error (BIT Word).

RESET REMOTE TERMINAL (01000)

MESSAGE SEQUENCE = RESET REMOTE TERMINAL ⋆ STATUS

The BUS-65142 responds with status and internally resets. Transmitter shutdown, mode commands, BIT Word, and inhibit terminal flag commands will be reset. If the command was broadcast, the broadcast received bit is set and the status word is suppressed.

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Followed by Data Word.*** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. ***T/$\overline{R}$ bit Set to Zero.*** No status response. Bits set: message error (SW), T/R Error (BIT Word).
4. ***Zero T/$\overline{R}$ bit and Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), T/R Error (BIT Word).

RESERVED MODE CODES (01001-01111)

MESSAGE SEQUENCE = RESERVED MODE CODES ⋆ STATUS

The BUS-65142 responds with clear status and no data. If the command is illegalized through an optional PROM, the message error bit is set and only the status word is transmitted.

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Followed by Data Word.*** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. ***T/$\overline{R}$ bit Set to Zero.*** No status response. Bits set: message error (SW), Illegal Mode Code (BIT Word).
4. ***Zero T/$\overline{R}$ bit and Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code (BIT Word).

⋆ = Status response time

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TABLE 2. MODE CODES (CONTINUED)

TRANSMIT VECTOR WORD (10000)

MESSAGE SEQUENCE = TRANSMIT VECTOR WORD ⋆ STATUS VECTOR WORD

The BUS-65142 transmits a status word followed by a vector word.

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Followed by Data Word.*** No status response. Bits set: message error (SW), High Word Count (BIT Word).
3. ***T/$\overline{R}$ bit Set to Zero.*** No status response. Bits set: message error (SW), T/R Error, Low Word Count (BIT Word).
4. ***Zero T/$\overline{R}$ bit and Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, T/R Error, Low Word Count (BIT Word).
5. ***Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, (BIT Word).

SYNCHRONIZE WITH DATA WORD (10001)

MESSAGE SEQUENCE = SYNCHRONIZE DATA WORD ⋆ STATUS

The data word received following the command word is transferred to the RAM. The status word is then transmitted. If the command was broadcast, the broadcast received bit is set and status transmission is suppressed.

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Not Followed by Data Word.*** No status response. Bits set: message error (SW), Low Word Count (BIT Word).
3. ***Command Followed by too many Data Words.*** No status response. Bits set: message error (SW), High Word Count (BIT Word).
4. ***Command T/$\overline{R}$ bit Set to One.*** No status response. Bits set: message error (SW), T/R Error, High Word Count (BIT Word).
5. ***Command T/$\overline{R}$ bit Set to Zero and Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), High Word Count, T/R Error (BIT Word).

TRANSMIT LAST COMMAND (10010)

MESSAGE SEQUENCE = TRANSMIT LAST COMMAND ⋆ STATUS LAST COMMAND

The status and BIT word registers are not altered by this command. The SW contains the status from the previous command. The data word transmitted contains the previous valid command (providing it was not another TRANSMIT LAST COMMAND).

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Followed by Data Word.*** No status response. Bits set: message error (SW).
3. ***T/$\overline{R}$ bit Set to Zero.*** No status response. Bits set: message error (SW), T/R Error, Low Word Count (BIT Word).
4. ***Zero T/$\overline{R}$ bit and Broadcast Address.*** No status response. Bits set: message error (SW), Illegal Mode Code, T/R Error (BIT Word).
5. ***Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code (BIT Word).

TRANSMIT BIT WORD (10011)

MESSAGE SEQUENCE = TRANSMIT BIT WORD ⋆ STATUS BIT WORD

The BUS-65142 responds with status followed by the BIT word. The BIT word is not altered by this command; however, the next SW will reflect errors in this transmission.

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Followed by Data Word.*** No status response. Bit set: message error (SW).
3. ***T/$\overline{R}$ bit Set to Zero.*** No status response. Bits set: message error (SW), T/R Error, Low Word Count (BIT Word).
4. ***Zero T/$\overline{R}$ bit and Broadcast Address.*** No status response. Bits set: message error (SW), Illegal Mode Code, T/R Error, Low Word Count (BIT Word).
5. ***Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code (BIT Word).

⋆ = Status response time

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PIN FUNCTION TABLE		
PIN	**FUNCTION**	**DESCRIPTION**
1	A9	Latched output of the most significant bit (MSB) in the subaddress field of the command word.
2	A7	Latched output of the third most significant bit in the subaddress field of the command word.
3	A5	Latched output of the least significant bit (LSB) in the subaddress field of the command word.
4	DB1	Bi-directional parallel data bus Bit 1
5	DB3	Bi-directional parallel data bus Bit 3
6	DB5	Bi-directional parallel data bus Bit 5
7	DB7	Bi-directional parallel data bus Bit 7
8	DB9	Bi-directional parallel data bus Bit 9
9	DB11	Bi-directional parallel data bus Bit 11
10	DB13	Bi-directional parallel data bus Bit 13
11	DB15	Bi-directional parallel data bus Bit 15 (MSB)
12	BRO ENA	Broadcast enable – when HIGH, this input allows recognition of an RT address of all ones in the command word as a broadcast message. When LOW, it prevents response to RT address 31 unless it was the assigned terminal address.
13	ADDRE	Input of the MSB of the assigned terminal address.
14	ADDRC	Input of the 3rd MSB of the assigned terminal address.
15	ADDRA	Input of the LSB of the assigned terminal address.
16	$\overline{\text{RTADERR}}$	Output signal used to inform subsystem of an address parity error. If LOW, indicates parity error and the RT will not respond to any command address to a single terminal. It will respond to broadcast commands if BRO ENA is HIGH.
17	$\overline{\text{TXDATA B}}$	LOW output to the primary side of the coupling transformer that connects to the B channel of the 1553 Bus.
18	NC	
19	GND B	Power supply return connection for the B channel transceiver.
20	RXDATA B	Input from the HIGH side of the primary side of the coupling transformer that connects to the B channel of the 1553 Bus.
21	A3	Multiplexed address line output. When INCMD is LOW or A6 thru A10 are all zeroes or all ones (Mode Command), it represents the latched output of the 2nd MSB in the word count field of the command word. When INCMD is HIGH and A6 thru A10 are not all zeroes or all ones, it represents the 2ns MSB of the current word counter.
22	A1	Multiplexed address line output. When INCMD is LOW or A6 thru A10 are all zeroes or all ones (Mode Command), it represents the latched output of the 2nd LSB in the word count field of the command word. When INCMD is HIGH and A6 thru A10 are not all zeroes or all ones, it represents the 2nd LSB of the current word counter.

PIN FUNCTION TABLE		
PIN	**FUNCTION**	**DESCRIPTION**
23	$\overline{\text{DTGRT}}$	Data transfer grant – active LOW input signal from the subsystem that informs the RT, when $\overline{\text{DTREQ}}$ is asserted, to start the transfer. Once transfer is started, $\overline{\text{DTGRT}}$ can be removed.
24	INCMD	In Command – HIGH level output signal used to inform the subsystem that the RT is presently servicing a command.
25	$\overline{\text{HSFAIL}}$	Handshake Fail – output signal that goes LOW and stays LOW whenever the subsystem fails to supply $\overline{\text{DTGRT}}$ in time to do a successful transfer. Cleared by the next $\overline{\text{NBGT}}$.
26	$\overline{\text{DTSTR}}$	A LOW level output pulse (166ns) present in the middle of every data word transfer over the parallel data bus. Used to latch or strobe the data into memory, FIFOs, registers, etc. Recommend using the rising edge to clock data in.
27	(DAT/$\overline{\text{CMD}}$)	Address line output that is LOW whenever the command word is being transferred to the subsystem over the parallel data bus, and is HIGH whenever data words are being transferred.
28	$\overline{\text{RTFAIL}}$	Remote Terminal Failure — latched active LOW output signal to the subsystem to flag detection of a remote terminal continuous self-test failure. Also set if The Watchdog Timeout circuit is activated. Cleared by the start of the next message transmission (status word)and set if problem is again detected.
29	$\overline{\text{DTREQ}}$	Data Transfer Request – active LOW output signal to the subsystem indicating that the RT has data for or needs data from the subsystem and requests a data transfer over the parallel data bus. Will stay LOW until transfer is completed or transfer timeout has occurred.
30	$\overline{\text{ADBC}}$	Accept Dynamic Bus Control – active LOW input signal from subsystem used to set the Dynamic Bus Control Acceptance bit in the status register if the command word was a valid, legal mode command for dynamic bus control.
31	TEST 2	Factory test point output – DO NOT USE. (see note 1)*
32	A10 (T/$\overline{\text{R}}$)	Latched output of the T/R bit in the command word.
33	$\overline{\text{ILLCMD}}$	Illegal Command – Active LOW input signal from the subsystem, strobed in on the rising edge of INCMD. Used to define the command word as illegal and to set the message error bit in the status register.
34	$\overline{\text{SRQ}}$	Subsystem Service Request – Input from the subsystem used to control the Service Request Bit in the status register. If LOW when the status word is updated, the Service Request Bit will be set; if HIGH, it will be cleared.
35	$\overline{\text{BITEN}}$	Built-in-Test Word Enable – LOW level output pulse (.5μsec), present when the built-in-test word is enabled on the parallel data bus.
36	$\overline{\text{RXDATA A}}$	Input from the LOW side of the primary side of the coupling transformer that connects to the A Channel of the 1553 Bus.
37	+5VA	+5 volt input power supply connection for the A channel transceiver.

* See notes at end of table.

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PIN FUNCTION TABLE		
PIN	FUNCTION	DESCRIPTION
38	−15VA	−15 volt input power supply connection for the A Channel transceiver.
39	TXDATA A	HIGH output to the primary side of the coupling transformer that connects to the A channel of the 1553 Bus.
40	$\overline{\text{NBGT}}$	New Bus Grant – LOW level output pulse (166 ns) used to indicate the start of a new protocol sequence in response to the command word just received.
41	A8	Latched output of the 2nd MSB in the subaddress field of the command word.
42	A6	Latched output of the 2nd LSB in the subaddress field of the command word.
43	DB0	Bidirectional parallel data bus Bit 0 (LSB)
44	DB2	Bidirectional parallel data bus Bit 2
45	DB4	Bidirectional parallel data bus Bit 4
46	DB6	Bidirectional parallel data bus Bit 6
47	DB8	Bidirectional parallel data bus Bit 8
48	DB10	Bidirectional parallel data bus Bit 10
49	DB12	Bidirectional parallel data bus Bit 12
50	DB14	Bidirectional parallel data bus Bit 14
51	+5V	+5 Volt input power supply connection for RTU digital logic section.
52	GND	Power supply return for RTU digital logic section.
53	ADDRD	Input of the 2nd MSB of the assigned terminal address.
54	ADDRB	Input of the 2nd LSB of the assigned terminal address.
55	ADDRP	Input of Address Parity Bit. The combination of assigned terminal address and ADDRP must be odd parity for the RT to work.
56	TXDATA B	HIGH, output to the primary side of the coupling transformer that connects to the B Channel of the 1553 Bus.
57	−15VB	−15 volt input power supply connection for the B channel transceiver.
58	+5VB	+5 volt input power supply connection for the B channel transceiver.
59	$\overline{\text{RXDATA B}}$	Input from the LOW side of the primary side of the primary side of the coupling transformer that connects to the B Channel of the 1553 Bus.
60	A2	Multiplexed address line output. When INCMD is LOW or A6 thru A10 are all zeroes or all ones (Mode Command),it represents the latched output of the 3rd MSB in the word count field of the command word. When INCMD is HIGH and A6 thru A10 are not all zeroes or all ones, it represents the 3rd MSB of the current word counter.
61	A0	Multiplexed address line output. When INCMD is LOW or A6 thru A10 are all zeroes or all ones (Mode Command), it represents the latched output of the LSB in the word count field of the command word. When INCMD is HIGH and A6 thru A10 are not all zeroes or all ones, it represents the LSB of the current word counter.
62	$\overline{\text{DTACK}}$	Data Transfer Acknowledge – active LOW output signal during data transfers to or from the subsystem indicating the RTU has received the $\overline{\text{DTGRT}}$ in response to $\overline{\text{DTREQ}}$ and is presently doing the transfer. Can be connected directly to pin 67 ($\overline{\text{BUF ENA}}$) for control of tri-state data buffers; and to tri-state address buffer control lines, if they are used.

PIN FUNCTION TABLE		
PIN	FUNCTION	DESCRIPTION
63	A4	Multiplexed address line output. When INCMD is LOW or A6 thru A10 are all zeroes or all ones (Mode Command), it represents the latched output of the MSB in the word count field of the command word. When INCMD is HIGH and A6 thru A10 are not all zeroes or all ones, it represents the MSB of the current word counter.
64	R/$\overline{\text{W}}$	Read/$\overline{\text{Write}}$ – output signal that controls the direction of the internal data bus buffers. Normally, the signal is LOW and the buffers drive the data bus. When data is needed from the subsystem, it goes HIGH to turn the buffers around and the RT now appears as an input The signal is HIGH only when $\overline{\text{DTREQ}}$ is active (LOW).
65	$\overline{\text{GBR}}$	Good Block Received – LOW level output pulse (.5μsec) used to flag the subsystem that a valid, legal, non-mode receive command with the correct number of data words has been received without a message error and successfully transferred to the subsystem.
66	16MHz IN	16MHz Clock Input – input for the master clock used to run RTU circuits.
67	$\overline{\text{BUF ENA}}$	Buffer Enable – input used to enable or tri-state the internal data bus buffers when they are driving the bus. When LOW, the data bus buffers are enabled. Could be connected to $\overline{\text{DTACK}}$ (Pin 62) if RT is sharing the same data bus as the subsystem. (see note 2)*
68	$\overline{\text{RESET}}$	Input resets entire RT when LOW.
69	$\overline{\text{RTFLAG}}$	Remote Terminal Flag – input signal used to control the terminal flag bit in the status register. If LOW when the status word is updated, the terminal flag bit would be set; if HIGH, it would be cleared. Normally connected to $\overline{\text{RTFAIL}}$ (Pin 28).
70	TEST 1	Watchdog Timeout test point – DO NOT USE. (see note 3)* (input)
71	$\overline{\text{BUSY}}$	Subsystem Busy – input from the subsystem used to control the busy bit in the status register. If LOW when the status word is updated, the busy bit will be set; if HIGH, it will be cleared. If the busy bit is set in the status register, no data will be requested from the subsystem in response to a transmit command. On receive commands, data will still be transferred to subsystem.
72	$\overline{\text{SSFLAG}}$	Subsystem Flag – input from the subsystem used to control the subsystem flag bit in the status register. If LOW when the status word is updated, the subsystem flag will be set; if HIGH, it will be cleared.
73	$\overline{\text{ME}}$	Message Error – output signal that goes LOW and stays LOW whenever there is a format or word error with the received message over the 1553 Data Bus. Cleared by the next $\overline{\text{NBGT}}$.
74	RXDATA A	Input from the HIGH side of the primary side of the coupling transformer that connects to the A channel of the 1553 Bus.
75	GNDA	Power supply return connection for the A Channel transceiver.
76	NC	
77	$\overline{\text{TXDATA A}}$	LOW output to the primary side of the coupling transformer that connects to the A channel of the 1553 Bus.
78	$\overline{\text{STATEN}}$	Status Word Enable – LOW level active output signal present when the status word is enabled on the parallel data bus.

* See notes at end of table.

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TABLE 2. MODE CODES (CONTINUED)

SELECTED TRANSMITTER SHUTDOWN (10100)

MESSAGE SEQUENCE = TRANSMITTER SHUTDOWN DATA ⋆ STATUS

The data word received is transferred to the subsystem and status is transmitted. No other action is taken by the BUS-65142. If the command was broadcast, the broadcast received bit is set and status transmission suppressed. Intended for use with RTs with more than one dual redundant channel.

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Not Followed by Data Word.*** No status response. Bits set: message error (SW), High Word Count, Illegal Mode Code (BIT Word).
3. ***Command Followed by too many Data Words.*** No status response. Bits set: message error (SW), Low Word Count, Illegal Mode Code (BIT Word).
4. ***Command T/$\overline{R}$ bit Set to One.*** No status response. Bits set: message error (SW), Illegal Mode Code, High Word Count (BIT Word).
5. ***Command T/$\overline{R}$ bit Set to One and Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, High Word Count (BIT Word).

OVERRIDE SELECTED TRANSMITTER SHUTDOWN (10101)

MESSAGE SEQUENCE = TRANSMITTER SHUTDOWN DATA ⋆ STATUS

The data word received after the command word is transferred to the subsystem. No other action is taken by the BUS-65142. If the command was broadcast, the broadcast received bit is set and status transmission suppressed.

ERROR CONDITIONS

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Not Followed by Data Word.*** No status response. Bits set: message error (SW), Low Word Count, Illegal Mode Code (BIT Word).
3. ***Command Followed by too many Data Words.*** No status response. Bits set: message error (SW), High Word Count, Illegal Mode Code (BIT Word).
4. ***Command T/$\overline{R}$ bit Set to One.*** No status response. Bits set: message error (SW), Illegal Mode Code, High Word Count (BIT Word).
5. ***Command T/$\overline{R}$ bit Set to One and Broadcast Address.*** No status response. Bits set: message error, broadcast received (SW), Illegal Mode Code, High Word Count, T/R Error (BIT Word).

RESERVED MODE CODES (10110 - 11111)

MESSAGE SEQUENCE = RESERVED MODE CODE (T/R = 1) ⋆ STATUS
RESERVED MODE CODE (T/R = 0) ⋆ STATUS

If Valid (T/R = 0)

The BUS-65142 responds with status. If the command was broadcast, the broadcast received bit is set and status transmission suppressed. If the command is illegalized through an optional PROM, the message error bit is set and only the status word is transmitted.

If Invalid (T/R = 1)

Respond with status and 1 data word.

ERROR CONDITIONS (T/R = 1)

1. ***Invalid Command.*** No response, command ignored.
2. ***Command Followed by Data Word.*** No status response. Bits set: message error (SW), High Word Count, Illegal Mode Code (BIT Word).

ERROR CONDITIONS (T/R = 0)

1. ***Invalid Command.*** No response, command ignored.
2. ***Command not Followed by Contiguous Data Word.*** No status response. Bits set: message error (SW), Low Word Count, Illegal Mode Code (BIT Word).
3. ***Command Followed by too many Data Words.*** No status response. Bits set: message error (SW), High Word Count, Illegal Mode Code (BIT Word).

UNDEFINED MODE CODES
(T/R = 0, MODE CODE 00000 TO 01111)

No Response, set message error bit.

⋆ = Status response time

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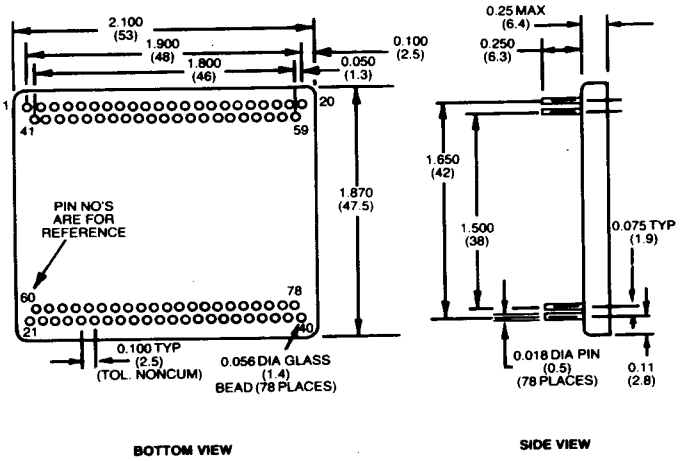
PIN FUNCTION TABLE NOTES:

1: PIN 31 – FACTORY TEST POINT OUTPUT
This pin provides the output of the BUS-65142 BIT Comparison output. It indicates the loop test results for every word transmitted by the BUS-65142. A test can be performed by actioning the RTU to transmit while the test fixture opens the receiver lines to force an error condition. A logic 1 (high) indicates the loop test passed. Normally this pin is left open.

2: PIN 67 – $\overline{\text{BUF ENA}}$
This pin is typically tied to $\overline{\text{DTACK}}$, causing the BUS-65142 to drive the shared data bus only while $\overline{\text{DTACK}}$ is active. If desired, $\overline{\text{BUF ENA}}$ can be grounded. The data will remain latched on the data bus pins for 18μs from $\overline{\text{DTSRB}}$ and 3.5μs for the last word of a message as the device's status word or BIT word is transferred to the BC ($\overline{\text{STATEN}}$ or $\overline{\text{BITEN}}$ low). Once the STATUS or BIT Word transfer is complete, the data bus will automatically again contain the last data word. The BUS-65142 will automatically switch the direction of the internal buffers during a transmit operation.

3: PIN 70 – TEST 1
This test allows the user to force the active channel to transmit indefinitely, in order to test the built in Watchdog Timer feature of the BUS-65142. When this pin is grounded and the active channel is stimulated with a valid transmit command, the BUS-65142 will respond with a status word and contiguous data (last data word loaded or STATUS WORD if none is loaded) until the built-in time-out occurs. Normally this pin is left open or an optional pull-up can be used.



Note: Dimensions are in inches (millimeters).

FIGURE 7. BUS-65142 MECHANICAL OUTLINE (DDIP)

ORDERING INFORMATION

BUS-65142-883

- Reliability Grade:
  - 883B = Fully compliant with MIL-STD-883.
  - B = Screened to MIL-STD-883 but without QCI testing.
- Power Supply Option & Packaging
  - 2 = −15VDC DDIP
  - 3 = −12VDC DDIP
  - 4 = −15VDC Flatpack
  - 5 = −12VDC Flatpack

Mating Data Bus Transformers:
for BUS-65142 use DDC BUS-25679
for BUS-65143 use DDC BUS-29854

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